

What is claimed

1. A method of operating a receiver apparatus to generate soft values ^{from} ~~form~~ a set of complex values communicated to said receiver apparatus, the method comprising operating said apparatus to perform the steps of:

4. a) receiving a first set of complex values, said first set of complex values being received complex symbol values obtained from signals communicated over a channel;
6. b) receiving a set of soft bits, said soft bits corresponding to said complex symbol values;
7. c) performing a complex multiplication operation on each of at least some of said first set of complex values to generate at least some elements of a second set of complex values, the multiplication operation performed on each individual one of said set of at least some of said first set of complex values including multiplying said individual complex values by a complex value determined from at least some of said soft bits;
12. d) summing said complex values in said second set of complex values to generate a complex sum, said complex sum being a complex value;
14. e) generating a third set of complex values, said third set having the same number of elements as said first set of complex values, by separately subtracting from said complex sum one of said second set of complex values, each separate subtraction generating one of said third set of complex values; and
18. f) multiplying each element of said first set of complex values with the conjugate of a complex value from said third set to generate a fourth set of complex values, said fourth set having the same number of elements as the first and second sets, said complex values in said fourth set being generated soft symbol values.

1. 2. The method of claim 1, wherein said received set of soft values is generated from the output of a decoder.

1. 3. The method of claim 1, wherein said separate subtractions performed in said step of generating a third set of complex values are performed sequentially.

1. 4. The method of claim 1, wherein there are at least two soft bits per received complex symbol value.

1 5. The method of claim 1, wherein there are at least 3 soft bits per received complex
2 symbol value.

1 6. The method of claim 1, wherein one of the received complex symbol values is
2 unmodified in phase by said step of performing said complex multiplication operation on each
3 of at least some of said first set of complex values.

1 7. The method of claim 6, wherein said complex symbol value that is unmodified in phase
2 occurs in a preselected location within the first set of received complex symbol values.

1 8. The method of claim 6, wherein for said complex symbol value that is unmodified in
2 phase, the multiplication is known and independent of soft bits.

1 9. The method of claim 6, wherein said complex symbol value that is unmodified in phase
2 is a pilot symbol value.

1 10. The method of claim 6, wherein said complex symbol value that is unmodified in phase
2 is a known symbol value representing a pseudo pilot symbol.

1 11. The method of claim 1, further comprising:
2 performing a soft input soft output decoding operation on said soft symbol values to
3 generate additional soft bits.

1 12. The method of claim 11, further comprising:
2 using said generated additional soft bits to process another set of complex symbol values.

1 13. The method of claim 11, wherein said soft input soft output decoding operation is
2 performed by a low density parity check decoder.

1 14. The method of claim 11, wherein said soft input soft output decoding operation is
2 performed by a turbo decoder.

1 15. The method of claim 1, wherein said first set of complex symbol values are produced by
2 an OFDM modulated communications system.

1 16. The method of claim 1, further comprising:
2 storing each of the generated second set of complex symbol values for a predetermined
3 time, said subtracting using symbol values from said second set which have been stored for said
4 predetermined time.

1 17. The method of claim 16, further comprising:
2 storing each of the first set of complex symbol values for a second predetermined time,
3 said second predetermined time being longer than the first predetermined time; and
4 wherein said first complex symbol values multiplied with said third complex symbol
5 values have been delayed for said second predetermined time.

1 18. The method of claim 5, wherein said complex multiplication operation on each of at least
2 some of said first set of complex values is performed by performing no more than two shift
3 operations and no more than one addition operation.

1 19. The method of claim 1, wherein the communication signal is block-coherent
2 communication signal.

1 20. The method of claim 1, wherein one of the received complex symbol values is modified
2 in phase by said step of performing said complex multiplication operation on each of at least
3 some of said first set of complex values by a fixed preselected amount.

1 21. The method of claim 20, wherein said complex symbol value that is modified in phase
2 by a fixed preselected amount occurs in a preselected location within the first set of received
3 complex symbol values.

1 22. The method of claim 20, wherein for said complex symbol value that is modified in
2 phase by a fixed preselected amount, the multiplication is known and independent of soft bits.

1 23. A apparatus for generating soft values ^{from} a set of complex values, the apparatus
2 comprising:

3 a first complex multiplier including:

4 i) a first input for receiving a first set of complex values, said first set of complex
5 values being received complex symbol values obtained from signals
6 communicated over a channel;
7 ii) a second input for receiving a set of soft bits, said soft bits corresponding to
8 said complex symbol values; and
9 iii) circuitry for performing a complex multiplication operation on each of at least
10 some of said first set of complex values to generate at least some elements of a
11 second set of complex values, the multiplication operation performed on each
12 individual one of said set of at least some of said first set of complex values
13 including multiplying said individual complex values by a complex value
14 determined from at least some of said soft bits;

15 a summer coupled to said first complex multiplier for summing said complex values in
16 said second set of complex values to generate a complex sum, said complex sum being a
17 complex value;

18 means for generating a third set of complex values, said third set having the same
19 number of elements as said first set of complex values, by separately subtracting from said
20 complex sum one of said second set of complex values, each separate subtraction generating one
21 of said third set of complex values; and

22 means for multiplying each element of said first set of complex values with the conjugate
23 of a complex value from said third set to generate a fourth set of complex values, said fourth set
24 having the same number of elements as the first and second sets, said complex values in said
25 fourth set being generated soft symbol values.

1 24. The apparatus of claim 23, further comprising:

2 a decoder which generates soft output values, said decoder being coupled to said first
3 input of said first complex multiplier.

1 25. The apparatus claim 23, wherein said means for generating a third set of complex values,
2 includes a delay line for delaying complex values included in said second set of complex values
3 and a subtractor coupled to said delay line.

1 26. The apparatus of claim 23, wherein there are at least two soft bits per received complex
2 symbol value.

1 27. The apparatus of claim 23, wherein said means for multiplying each element of said first
2 set of complex values with the conjugate of a complex value from said third set to generate a
3 fourth set of complex values includes:

4 a conjugate circuit; and
5 a second complex multiplier.